Listing of Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

1. (Currently amended) A method for controlling the access to all or part of the content of a first memory integrated with a microprocessor, the method comprising:

executing an access control algorithm contained in a second auxiliary memory using a priority-holding interrupt (PRIORIN); and

accessing the content of the first memory with the access control algorithm using at least one register of keys, ;and

applying at least one access control algorithm contained in a wherein the second auxiliary memory is distinct and separate from the first memory and using the content of at least one also integrated storage element and the content of the key register, the content of the auxiliary memory being programmable only once.

2. (Previously presented) The method of claim 1, wherein at least one sub-program authorizing the execution of a function of access to the first memory is contained in the auxiliary memory.

3. (Original) The method of claim 1, wherein the priority-holding interrupt (PRIORIN) is non-interruptible, even by itself.

4. (Original) The method of claim 1, wherein said priority-holding interrupt (PRIORIN) is generated provided that a signal (MODE) indicative of an access control operating mode is in an active state.

5. (Original) The method of claim 1, wherein said priority-holding interrupt (PRIORIN) can be generated upon occurrence of an interrupt request coming from the outside (EXTPRIORIN) of the integrated circuit or from the inside (INTPRIORIN).

6. (Previously presented) The method of claim 1, wherein said first memory is a program memory containing embarked functions.

7. (Currently amended) The method of claim 6, wherein said storage element is formed by the program memory the step of accessing the content of the first memory with the access control algorithm using at least one register of keys includes using the content of at least one integrated storage element along with the content of the key register.

8. (Currently amended) A circuit comprising: integrating

a microprocessor [[and]] integrated with at least one first memory, which includes :

a second auxiliary memory adapted to containing at least one sub-program enabling authorizing the execution of a function of access to said for accessing the content of the first memory, wherein said second auxiliary memory is distinct and separate from the first memory and the content of the auxiliary memory being programmable only once.

9. (Currently amended) The circuit of claim 8, further including means for selecting, at [[the]] an input of a memory interface of the microprocessor, a memory from among at least[[:]] said auxiliary memory[[;]] and said first memory, wherein

the selection of said first memory, otherwise that for the execution of a function that it contains, requiring an authorization from an algorithm contained in the auxiliary memory and

using the content of at least one ~~also~~ integrated storage element and the content of the key

register.

10. (Previously presented) The circuit of claim 9, wherein the first memory and the

storage element are one and the same program memory.

11. (Currently amended) The circuit of claim 8, <u>further</u> including means for generating a

priority-holding interrupt for executing said sub-program, ~~the priority-holding interrupt being~~

~~generated~~ provided that:

       a signal (MODE) indicative of an access-control operating mode is in an active

state;

       an access to the first memory has been requested otherwise than for a non-

interruptible execution of one of the functions that it contains; and

       an interrupt signal (EXTPRIORIN, INTPRIORIN) is active, <u>wherein</u> the resulting

priority-holding interrupt being non-interruptible~~, even by itself~~.

12.   (Canceled)